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APPLICATION

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TITLE: SHIFT REGISTER CHAIN FOR TRIMMING GENERATORS FOR AN INTEGRATED SEMICONDUCTOR APPARATUS

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"Shift register chain for trimming generators for an integrated semiconductor apparatus"

Description

The invention relates to an integrated semiconductor apparatus having trimmable generators, as claimed in claim 1.

Integrated semiconductor apparatuses typically have a large number of generators, which are integrated on-chip (on the chip). Generators such as these may, for example, be designed to produce an internal supply voltage, which is used internally in the chip, that is to say in the integrated semiconductor apparatus. Particularly in the case of semiconductor memories, for example DRAMs, on-chip voltages which are required in the memory are produced by voltage generators. Since the requirements which are placed on the production of such internal voltage supplies to the generators (minimum discrepancies between the emitted actual voltage and a desired nominal voltage) are becoming continuously more stringent, generator signals such as these must be "trimmed". During the trimming process, the generator signal, that is to say the output signal from a generator, is matched by means of trimming data as closely as possible to a desired reference signal or nominal signal. Trimming is particularly necessary since the components from which such generators are constructed are subject to parameter fluctuations which are caused by process fluctuations during the production process (for example the CMOS process).

Thus, the generators which must be trimmed must be measured, even at what is referred to as the wafer level,

in order to define the trimming data that is required for trimming. The defined trimming data is then stored in a nonvolatile memory, which is accommodated in a fuse block device. The fuse block device contains a large number of nonvolatile, programmable fuses, in which the trimming data can be stored in a nonvolatile form. In order to transmit the trimming data from the fuse block device to the generators, which may be distributed at different locations in the chip, lines must be provided, some of which must be wired transversely through the chip. Modern DRAM memories have a large number of trimming signals which pass transversely through the chip and which contribute to the overall chip width.

Against the background of the above disadvantages, one object of the invention is to specify an integrated semiconductor apparatus having trimmable generators, in which the transmission of the trimming signals does not significantly complicate the chip layout.

This object is achieved by an integrated semiconductor apparatus having the features stated in claim 1. Preferred embodiments are the subject matter of the dependent claims.

According to the invention, an integrated semiconductor apparatus comprises:

- a large number of generators for producing predetermined generator signals, with each of the generators having a trimming unit with a trimming signal input for receiving digital trimming data, and the trimming unit being designed for trimming the generator signals that are produced, as a function of the trimming data;
- at least one fuse block device having

-- a large number of fuses which are designed for nonvolatile storage of the trimming data for trimming the large number of generators,

-- a parallel/serial converter which is connected to the fuses and to a timer for signaling purposes and is designed to read the trimming data from the fuses in parallel and to emit it in serial form via a fuse block trimming output to the fuse block device in time with the timer;

in which

- each of the generators has a trimming signal output and a large number of memory flipflops which connect the trimming signal input of the generator to its trimming signal output, and
- the memory flipflops of the trimming units are connected to the fuse block trimming output in the form of a shift register chain for serial transmission of the trimming data from the fuse block device to the generators.

Thus, according to the invention, a shift register chain is used for serial transmission of the trimming data from the fuse block device to the individual generators. There is therefore no need to route a large number of trimming lines in parallel transversely through the chip. Only a single trimming data line is preferably provided, which passes through the large number of generators in the form of a chain from the fuse block trimming output. For this purpose, the trimming units of the generators have memory flipflops, which are arranged between a trimming signal input and a trimming signal output of the trimming units. The trimming data which is stored in the fuses of the fuse block device is read by the parallel/serial converter, and is emitted as a serial data stream in time with the timer, via the fuse block trimming output. After a predetermined number of shift cycles in the shift

register chain, the correct trimming data is available for the trimming units of the individual generators, so that the generator signals can be trimmed correctly.

The generator signals are preferably signals which are produced and required on-chip, and are emitted from the generator via a generator output. The expression trimming of these signals means matching of the (untrimmed) actual voltage to a desired (trimmed) nominal voltage. The final generator which is provided at the end of the shift register chain does not necessarily need to have a trimming signal output, since it need not be connected to any further generator.

The trimming signal output is preferably connected from one of the generators to the fuse block trimming output, and the trimming signal inputs of the other generators are each connected in the form of a chain to one, and only one, of the trimming signal outputs. Each trimming unit preferably has one, and only one, trimming signal input. A trimming signal input of one of the generators is connected to the fuse block trimming output. The trimming signal output of this generator is connected to a downstream trimming signal input of the next generator, so that the generators are connected to the fuse block device in the form of a chain.

The generators are preferably voltage generators and the generator signals are preferably output voltages, with the trimming units being designed for trimming the output voltage as a function of the trimming data. The generators may, for example, be what are referred to as charge pumps, which produce supply voltages required in the chip by "pumping" of externally applied voltages. Voltage generators such as these emit as the generator

signals output voltages which have to satisfy stringent specifications. During the process of trimming such output voltages, digital (binary) trimming data is supplied to the trimming units of such voltage generators, which can associate the binary trimming data with a predetermined voltage correction, for example by means of a table stored in the trimming units.

Alternatively, the generators are delay generators and the generator signals are signals which are delayed in time with respect to a reference signal, with the trimming units being designed for trimming the time delay of the time-delayed signal as a function of the trimming data. For example, the reference signal may be a clock signal, and the time-delayed signal may be a generator signal, which is delayed in time in a specific manner with respect to this clock signal. The magnitude or the duration of the time delay of the time-delayed signal with respect to the reference signal likewise has to satisfy stringent specifications for numerous applications, so that it must be trimmed by means of a trimming unit. The magnitude of the time delay can be adjusted via binary trimming data, which is supplied to the trimming unit, by means of a table which is stored in the trimming unit. For this purpose, the reference signal is fed into the generator.

The fuse block device preferably has a fuse block clock output for emitting the clock of the timer, and the fuse block clock output is connected to clock inputs of the generators for signaling purposes. This allows a shift register to be configured in a particularly simple manner, using time-division multiplexing. The clock with which the individual binary trimming data is in each case shifted further through one memory flipflop in the shift

register chain is in this embodiment supplied to the trimming units through a separate clock line.

As an alternative to the separate transfer of the clock signal from the fuse block device to the generators as just described, the parallel/serial converter can be designed to emit the trimming data in pulse-width modulated form. The serial data stream which is emitted from the parallel/serial converter via the fuse block trimming output is thus puse-width modulated (pulse-duration modulated). In the case of pulse-duration modulation, the binary data to be transmitted is coded by the duty ratio of the time periods between a high voltage value and a low voltage value, with a constant pulse repetition frequency. The clock signal can thus be derived in a known manner from the pulse-duration modulated signal, so that it need not be separately transmitted to the trimming units. This allows a further reduction in the wiring complexity between the fuse block device and the individual generators, since only a single trimming line (data line) advantageously need be provided for transmission of the trimming signals.

The fuses in the fuse block device are preferably electrically or laser-programmable.

The integrated semiconductor apparatus is preferably an integrated semiconductor memory, in particular a DRAM memory.

The invention can also equally be used for integrated logic circuits, for example for processors.

The invention will be described by way of example in the following text with reference to an accompanying drawing of one preferred embodiment, in which:

Figure 1 shows a schematic block diagram of one preferred embodiment of an integrated semiconductor apparatus having a shift register chain for generator trimming.

Figure 1 shows a highly simplified block diagram of a fuse block device 10 as well as generators G_A, G_B, ..., G_X. The fuse block device 10 has a large number of fuses 12, which are indicated in the form of a fuse box in Figure 1. The large number of fuses 12 are connected in parallel to a parallel input 14_D of a parallel/serial converter 14. The parallel/serial converter 14 receives a clock signal CLK from a timer 16, which is likewise arranged in the fuse block device 10. The parallel/serial converter 14 is driven by a control device 18, which has control inputs 20 which signal, for example, the start and end of a trimming cycle. The parallel/serial converter 14 loads the trimming data (which is stored in the fuses 12) via its input 14_D, and converts this trimming data to a serial binary trimming data stream at the clock rate CLK of the timer 16. The serial trimming data signal TRM is emitted from the fuse block device 10 via the fuse block trimming output 14_Q.

The generators G_A, G_B, ..., G_X are connected to the fuse block trimming output 14_Q in the form of a shift register chain. A shift register is a chain of memory flipflops, which make it possible to shift information which is applied to the input onward by one memory flipflop with each clock cycle. After passing through the chain, the information is produced at the output with a

delay, but otherwise unchanged. In this context, reference is made to the description of shift registers in "Halbleiter-Schaltungstechnik" [Semiconductor circuit technology] by U. Titze and Ch. Schenk, 12th edition, Springer-Verlag, Chapter 9.5, whose explanatory notes relating to shift registers are an integral component of the present application. The fuse block trimming output 14_Q is connected via a single trimming line to a trimming signal input 22_A of the generator G_A. Within the generator G_A there is a trimming unit which is not illustrated in any more detail but which has an m bits shift register with the trimming signals TRM<0>, TRM<1>, ..., TRM<m>. The m bits shift register of the generator G_A (and of the other generators) is illustrated enlarged, in a partial view, in the inset in Figure 1.

The serial trimming signal TRM is applied to an input connection D of a memory flipflop 24. Furthermore, the clock CLK from the timer 16 is supplied to the memory flipflop 24 externally via a clock input 26_A of the generator G_A. The generator G_A also has a trimming signal output 28_A, which is connected to the trimming signal input 22_B of the generator G_B. The shift register chain which is provided in the generator G_B has n bits. The trimming output 28_B of the generator G_B is connected to the trimming signal input 22_X of the next generator (which is not illustrated in any more detail). In this way, the shift register chain is continued as far as the generator G_X, which forms the last generator in the shift register chain and does not necessarily need to have a trimming signal output 28_X.

During operation, the binary serial trimming signal TRM is shifted, clocked in time with the clock CLK of the timer 16, by the memory flipflops 24 through all the

generators G_A, G_B, ..., G_X. After a number of clock cycles which corresponds to the total number of memory flipflops 24 for all the generators, the first emitted trimming signal bit is produced at the final data output TRM<0> of the last generator G_X, so that all the trimming signals have been transmitted to the trimming units correctly.

Since the transmission rate or the clock CLK is typically several tens of MHz, but the time constants for changes to the generator signals are several microseconds, the generators cannot follow the process during the single transmission of the trimming data when the chip is being started up. Correctly trimmed generator signals are not produced until the trimming data has been successfully transmitted.

While in the case of conventional trimming concepts, 40 to 50 trimming signals typically have to be routed transversely through the chip (each trimming unit typically has 3 to 6 binary inputs and there are typically 10 generators in each memory chip), the generator trimming by means of the shift register chain allows a considerable simplification to the design.

List of reference symbols

10	Fuse block device
12	Fuses
14	Parallel/serial converter
16	Timer
18	Control device
20	Control inputs
22_A	Trimming signal input of the generator A
22_B	Trimming signal input of the generator B
22_X	Trimming signal input of the generator X
24	Memory flipflop
26_A	Clock input of the generator A
26_B	Clock input of the generator B
26_X	Clock input of the generator X
28_A	Trimming signal output of the generator A
28_B	Trimming signal output of the generator B
28_X	Trimming signal output of the generator X
CLK	Clock signal
G_A	Generator A
G_B	Generator B
G_X	Generator X
TRM	Trimming signal
TRM<i>	Trimming data